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1. A method of calibrating a digital circuit, comprising:

receiving a calibration bit pattern at a first logic device;

storing said received calibration bit pattern at said first logic device;

using said stored first calibration pattern during subsequent calibration operations to adjust a relative timing of clock and data signals on at least one data path of said first logic device to produce a reliable detection of said calibration bit pattern.

2. A method as in claim 1 wherein said receiving of said calibration bit pattern is performed at a first data rate slower than a normal operating data rate at which said first logic device usually receives data.

3. A method as in claim 2 wherein said reliable detection of said calibration bit pattern is performed at a second data rate approximately equal to said normal operating data rate.

4. A method as in claim 3 wherein said second data rate is about an integer number of times as fast as said first data rate.

5. A method as in claim 3 wherein said second data rate is about four times as fast as said first data rate.

6. A method as in claim 3 wherein said second data rate is about eight times as fast as said first data rate.

7. A method as in claim 1 wherein said act of storing includes storing only every Nth bit of data received at said first logic device.

8. A method as in claim 1 wherein said act of storing includes storing every bit received at said first logic device, and said act of using said stored calibration bit pattern during subsequent calibration operations includes retrieving only every Nth bit stored during said act of storing.

9. A method as in claim 1 wherein said act of storing includes using a prefetch demultiplexer that stores only every Nth bit received.

10. A method as in claim 8 wherein said act of retrieving every Nth bit stored includes using a linear address counter to count only every Nth address of said received bits stored during said act of storing.

11. A method as in claim 8 wherein said act of retrieving every Nth bit stored includes using a test mode circuit to count only every Nth address of said received bits stored during said act of storing.

12. A method as in claim 2 wherein said receiving of said calibration bit pattern at said first data rate includes lowering a frequency of a clock signal used to synchronize said act of receiving.

13. A method as in claim 2 further comprising deactivating one of a delay locked loop (DLL) and phase locked loop (PLL) circuits at said first logic device at least during said act of receiving said calibration bit pattern.

14. A method as in claim 1 further comprising receiving a pattern input mode command at said first logic device prior to receiving said calibration bit pattern at said first logic device.

15. A method as in claim 14 wherein said receiving of said pattern input mode command is performed at a first data rate slower than a normal operating data rate of said first logic device.

16. A method as in claim 15 wherein said receiving of said pattern input mode command includes using data paths of said first logic device that normally operate at said first data rate.

17. A method as in claim 15 wherein said receiving of said pattern input mode command includes receiving said command N consecutive times on a command and address bus.

18. A method as in claim 17 wherein said pattern input mode command is a burst terminate command and N is an integer equal to 4.

19. A method as in claim 17 wherein said pattern input mode command is a burst terminate command and N is an integer equal to 6.

20. A method as in claim 1 wherein said receiving of said calibration bit pattern includes receiving said calibration bit pattern from a BIOS.

21. A method as in claim 1 wherein said receiving of said calibration bit pattern is performed using a READ/WRITE data bus connected to said first logic device.

22. A method as in claim 1 wherein said receiving of said calibration bit pattern is performed using a command and address bus connected to said first logic device.

23. A method as in claim 1, wherein said data path is an address path.

24. A method as in claim 1, wherein said data path is a command signal path.

25. A method as in claim 1, wherein said data path is a data bus signal path.

26. A method as in claim 1, wherein said data path is an input data line signal path.

27. A method as in claim 1, wherein said calibration method is performed at power-up and reset of said digital circuit.

28. A method of calibrating a digital circuit, comprising:

providing a first calibration bit pattern at a location external to a first logic device;

transmitting said first calibration pattern to said first logic device;

storing said transmitted first calibration pattern at said first logic device;

producing a first calibration signal by repeating said first calibration pattern;

applying said repeating first calibration signal to at least one data path of said first logic device; and

using said stored first calibration pattern, said applied first calibration signal and a clock signal at said first logic device to adjust a relative timing of clock and data signals on at least one data path of said first logic device to produce a reliable detection of said calibration bit pattern on said at least one data path.

29. A method as in claim 28 wherein said transmitting of said first calibration pattern is performed at a first data rate slower than a normal operating data rate at which said first logic device usually receives data.

30. A method as in claim 29 wherein said reliable detection of said first calibration pattern is performed at a second data rate approximately equal to said normal operating data rate.

31. A method as in claim 30 wherein said second data rate is approximately four times as fast as said first data rate.

32. A method as in claim 30 wherein said second data rate is approximately eight times as fast as said first data rate.

33. A method as in claim 28 wherein said act of storing includes storing only every Nth bit transmitted to said first logic device.

34. A method as in claim 28 wherein said act of storing includes storing every bit transmitted to said first logic device, and said act of producing said repeating first calibration signal includes retrieving only every Nth bit stored during said act of storing.

35. A method as in claim 28 wherein said act of storing includes using a prefetch demultiplexer that shifts only every Nth bit into storage.

36. A method as in claim 28 wherein said act of producing said repeating first calibration signal includes using a linear address counter to count only every Nth address of said transmitted bits stored during said act of storing.

37. A method as in claim 28 wherein said act of producing said repeating first calibration signal includes using a test mode circuit to count only every Nth address of said transmitted bits stored during said act of storing.

38. A method as in claim 29 wherein said transmitting of said first calibration pattern at said first data rate includes lowering a frequency of a clock signal used to synchronize said act of transmitting.

39. A method as in claim 28 further comprising deactivating one of a delay locked loop (DLL) and phase locked loop (PLL) circuits at said second logic device at least during said act of transmitting said first calibration pattern.

40. A method as in claim 28 wherein said transmitting of said first calibration pattern at said first data rate includes transmitting each bit of said first calibration pattern N consecutive times.

41. A method as in claim 40 wherein N is an integer equal to 4.

42. A method as in claim 38 further comprising deactivating one of a delay locked loop (DLL) and phase locked loop (PLL) circuits at said second logic device at least during said act of transmitting of said first calibration pattern.

43. A method as in claim 28 further comprising transmitting a pattern input mode command to said first logic device prior to transmitting said first calibration pattern to said first logic device.

44. A method as in claim 43 wherein said transmitting of said pattern input mode command is performed at a first data rate slower than a normal operating data rate of said digital circuit.

45. A method as in claim 44 wherein said transmitting of said pattern input mode command includes using data paths of said first logic device that normally operate at said first data rate.

46. A method as in claim 43 wherein said transmitting of said pattern input mode command includes repeating a command N consecutive times on a command or address bus.

47. A method as in claim 46 wherein said repeated command is a burst terminate command and N is an integer equal to 4.

48. A method as in claim 46 wherein said repeated command is a burst terminate command and N is an integer equal to 6.

49. A method as in claim 28 wherein said providing of said first calibration pattern includes retrieving said first calibration pattern from a BIOS.

50. A method as in claim 28 wherein said transmitting of said first calibration pattern is performed using a READ/WRITE data bus connected to said first logic device.

51. A method as in claim 28 wherein said transmitting of said first calibration pattern is performed using a command or address bus connected to said first logic device.

52. A method as in claim 28, wherein said data path is an address path.

53. A method as in claim 28, wherein said data path is a command signal path.

54. A method as in claim 28, wherein said data path is a data bus signal path.

55. A method as in claim 28, wherein said data path is an input data line signal path.

56. A method as in claim 28, wherein said calibration method is performed at power-up and reset of said digital circuit.

57. A method as in claim 28, wherein said clock signal clocks data on at least one of a rising or falling edge of said clock signal.

58. A method as in claim 28, wherein said clock signal clocks data on both rising and falling edges of said clock signal.

59. A method of calibrating a digital circuit, comprising:

providing a first calibration bit pattern to a first logic device;

transmitting said first calibration pattern from said first logic device to a second logic device;

storing said transmitted first calibration pattern at said second logic device;

producing a first calibration signal by repeating said first calibration pattern at said second logic device;

applying said repeating first calibration signal to at least one data path of said first logic device; and

using said provided first calibration pattern, said applied first calibration signal and a clock signal at said first logic device to adjust a relative timing of clock and data signals on at least one data path of said first logic device to produce a reliable detection of said calibration bit pattern on said at least one data path.

60. A method as in claim 59, further comprising producing a repeating second calibration signal that includes said first calibration pattern at said first logic device, applying said second calibration signal to at least one data path of said second logic device, and using said stored first calibration pattern, said applied second calibration signal and a clock signal at said second logic device to adjust a relative timing of clock and data signals on at least one data path of said second logic device to produce a reliable detection of said calibration bit pattern on said at least one data path of said second logic device.

61. A method as in claim 59 wherein said transmitting of said first calibration pattern to said second logic device is performed at a first data rate slower than a normal operating data rate of said digital circuit, and said applying of said first calibration signal to said at least one data path of said first logic device is performed at a second data rate approximately equal to said normal operating data rate.

62. A method as in claim 60 wherein said transmitting of said first calibration pattern to said second logic device is performed at a first data rate slower than a normal operating data rate of said digital circuit, and said applying of said first calibration signal to said at least one data path of said first logic device is

performed at a second data rate approximately equal to said normal operating data rate.

63. A method as in claim 62 wherein said applying of said second calibration signal to said at least one data path of said second logic device is performed at said second data rate approximately equal to said normal operating data rate.

64. A method as in claim 59 wherein said act of storing includes storing only every Nth bit transmitted to said second logic device.

65. A method as in claim 59 wherein said act of storing includes storing every bit transmitted to said second logic device, and said act of producing said repeating first calibration signal includes retrieving only every Nth bit stored during said act of storing.

66. A method as in claim 59 wherein said act of storing includes using a prefetch demultiplexer that shifts only every Nth bit into storage.

67. A method as in claim 59 wherein said act of producing said repeating first calibration signal includes using a linear address counter to count only every Nth address of said transmitted bits stored during said act of storing.

68. A method as in claim 59 wherein said act of producing said repeating first calibration signal includes using a test mode circuit to count only every Nth address of said transmitted bits stored during said act of storing.

69. A method as in claim 61 wherein said transmitting of said first calibration pattern at said first data rate includes lowering a frequency of a clock signal used to synchronize said act of transmitting.

70. A method as in claim 59 further comprising deactivating one of a delay locked loop (DLL) and phase locked loop (PLL) circuits at said second logic device at least during said act of transmitting said first calibration pattern.

71. A method as in claim 61 wherein said transmitting of said first calibration pattern at said first data rate includes transmitting each bit of said first calibration pattern N consecutive times.

72. A method as in claim 71 wherein N is an integer equal to 4.

73. A method as in claim 71 further comprising deactivating one of a delay locked loop (DLL) and phase locked loop (PLL) circuits at said second logic device at least during said act of transmitting of said first calibration pattern.

74. A method as in claim 61 wherein said second data rate is approximately four times as fast as said first data rate.

75. A method as in claim 61 wherein said second data rate is approximately eight times as fast as said first data rate.

76. A method as in claim 59 further comprising transmitting a pattern input mode command to at least said second logic device prior to transmitting said first calibration pattern to said second logic device.

77. A method as in claim 76 wherein said transmitting of said pattern input mode command is performed at a first data rate slower than a normal operating data rate of said digital circuit.

78. A method as in claim 77 wherein said transmitting of said pattern input mode command includes using data paths of said second logic device that normally operate at said first data rate.

79. A method as in claim 76 wherein said transmitting of said pattern input mode command includes repeating a command N consecutive times on said command or address bus.

80. A method as in claim 79 wherein said repeated command is a burst terminate command and N is an integer equal to 4.

81. A method as in claim 79 wherein said repeated command is a burst terminate command and N is an integer equal to 6.

82. A method as in claim 59 wherein said transmitting of said first calibration pattern to said second logic device is performed using a serial link.

83. A method as in claim 59 wherein said applying of said first calibration signal to said at least one signal path of said first logic device is performed at a data rate slower than or approximately equal to a normal operating data rate of said digital circuit.

84. A method as in claim 59 wherein said providing of said first calibration pattern includes loading said first calibration pattern from a BIOS.

85. A method as in claim 59 wherein said providing of said first calibration pattern includes loading said first calibration pattern from a ROM.

86. A method as in claim 59 wherein said providing of said first calibration pattern includes loading said first calibration pattern using a bus.

87. A method as in claim 59 wherein said providing of said first calibration pattern includes transmitting said first calibration pattern over a network connection.

88. A method as in claim 59 wherein said transmitting of said first calibration pattern to said second logic device includes transmitting said first calibration pattern over a network connection.

89. A method as in claim 59 wherein said transmitting of said first calibration pattern to said second logic device is performed using a command or address bus.

90. A method as in claim 59 wherein said transmitting of said first calibration pattern to said second logic device is performed using a command or address bus, and said applying of said first calibration signal to said at least one signal path of said first logic device is performed using a READ/WRITE data bus.

91. A method as in claim 59 wherein said transmitting of said first calibration pattern to said second logic device is performed using a first data bus, and said applying of said first calibration signal to said at least one signal path of said first logic device is performed using a second data bus.

92. A method as in claim 59 wherein said transmitting of said first calibration pattern to said second logic device is performed using a first portion of a bus, and said applying of said first calibration signal to said at least one signal path of said first logic device is performed using a second portion of said bus different from said first portion of said bus.

93. A method as in claim 59 wherein said providing of said first calibration pattern includes using cache memory to temporarily store said first calibration pattern.

94. A method as in claim 59 wherein said storing of said transmitted first calibration pattern includes using cache memory to temporarily store said transmitted first calibration pattern.

95. A method as in claim 59 wherein said first logic device is a memory controller and said second logic device is a memory device.

96. A method as in claim 59 wherein said first logic device is a bus master and said second logic device is a bus slave.

97. A method as in claim 59 wherein said first logic device is a DRAM controller and said second logic device is a DRAM memory device.

98. A method as in claim 59 wherein said first logic device is a microprocessor and said second logic device is a control logic chip.

99. A method as in claim 59 wherein said first logic device is one of a network hub and switch and said second logic device is an adapter card.

100. A method as in claim 59 wherein said signal path is an address signal path.

101. A method as in claim 59 wherein said signal path is a command signal path.

102. A method as in claim 59 wherein said signal path is a data bus signal path.

103. A method as in claim 59 wherein said signal path is an input data line signal path.

104. A method as in claim 59 wherein said calibration method is performed at power-up and reset of said digital circuit.

105. A digital circuit for calibrating an incoming signal path of a logic device, comprising:

an incoming pattern signal path;

a pattern storage device;

at least one incoming data signal path;

at least one variable delay circuit, respectively provided in said incoming data signal path or a clock signal path;

a control logic circuit connected to receive a calibration pattern signal including a calibration bit pattern on said incoming pattern signal path and store said calibration bit pattern in said pattern storage device, said control logic circuit subsequently using said stored calibration bit pattern and a clock signal during calibration operations to adjust said variable delay circuit to a delay value which produces a reliable detection of said stored calibration bit pattern within a calibration data signal received on said at least one incoming data signal path.

106. The digital circuit of claim 105, further comprising a comparator circuit which compares bit patterns within said calibration data signal received on said at least one incoming data signal path with said stored calibration bit pattern during calibration operations, said control logic circuit using an output of said comparator circuit to determine said reliable detection of said calibration bit pattern within said calibration data signal.

107. The digital circuit of claim 105 wherein said calibration pattern signal is received on said incoming pattern signal path at a first data rate slower than a normal operating data rate of said digital circuit.

108. The digital circuit of claim 107 wherein said calibration data signal is received on said at least one incoming data signal path at a second data rate approximately equal to said normal operating rate of said digital circuit.

109. The digital circuit of claim 107 wherein said calibration data signal is received on said at least one incoming data signal path at a second data rate slower than or approximately equal to said normal operating rate of said digital circuit.

110. The digital circuit of claim 107 wherein said normal operating data rate of said digital circuit is about an integer number of times as fast as said first data rate.

111. The digital circuit of claim 110 wherein said normal operating data rate of said digital circuit is about four times as fast as said first data rate.

112. The digital circuit of claim 110 wherein said normal operating data rate of said digital circuit is about eight times as fast as said first data rate.

113. The digital circuit of claim 105 wherein said calibration bit pattern is received from a data bus connected to said incoming pattern signal path.

114. The digital circuit of claim 105 wherein said calibration bit pattern is received from a command or address bus connected to said incoming pattern signal path.

115. The digital circuit of claim 105 wherein said at least one incoming data signal path is an address signal path.

116. The digital circuit of claim 105 wherein said at least one incoming data signal path is a command signal path.

117. The digital circuit of claim 105 wherein said at least one incoming data signal path is a data bus signal path.

118. The digital circuit of claim 105 wherein said at least one incoming data signal path is an input line signal path.

119. The digital circuit of claim 105 wherein said calibration bit pattern is received and calibration operations are performed at power-up and reset of said logic device.

120. The digital circuit of claim 105 wherein said clock signal clocks data on at least one of a rising or falling edge of said clock signal.

121. The digital circuit of claim 105 wherein said clock signal clocks data on both rising and falling edges of said clock signal.

122. A logic device, comprising:

an incoming pattern signal path;

a pattern storage device;

at least one incoming data signal path;

at least one variable delay circuit, respectively provided in said incoming data signal path or a clock signal path;

a control logic circuit connected to receive a calibration pattern signal including a calibration bit pattern on said incoming pattern signal path and store said calibration bit pattern in said pattern storage device, said control logic circuit subsequently using said stored calibration bit pattern and a clock signal during calibration operations to adjust said variable delay circuit to a delay value which produces a reliable detection of said stored calibration bit pattern within a calibration data signal received on said incoming data signal path.

123. The logic device of claim 122, further comprising a comparator circuit which compares bit patterns within said calibration data signal received on said at least one incoming data signal path with said stored calibration bit pattern during calibration operations, said control logic circuit using an output of said

comparator circuit to determine said reliable detection of said calibration bit pattern within said calibration data signal.

124. The logic device of claim 122 wherein said calibration pattern signal is received on said incoming pattern signal path at a first data rate slower than a normal operating data rate of said digital circuit.

125. The logic device of claim 124 wherein said calibration data signal is received on said at least one incoming data signal path at a second data rate approximately equal to said normal operating rate of said digital circuit.

126. The logic device of claim 124 wherein said calibration data signal is received on said at least one incoming data signal path at a second data rate slower than or approximately equal to said normal operating rate of said digital circuit.

127. The logic device of claim 124 wherein said normal operating data rate of said digital circuit is about an integer number of times as fast as said first data rate.

128. The logic device of claim 127 wherein said normal operating data rate of said digital circuit is about four times as fast as said first data rate.

129. The logic device of claim 127 wherein said normal operating data rate of said digital circuit is about eight times as fast as said first data rate.

130. The logic device of claim 122 wherein said calibration bit pattern is received from a data bus connected to said incoming pattern signal path.

131. The logic device of claim 122 wherein said calibration bit pattern is received from a command or address bus connected to said incoming pattern signal path.

132. The logic device of claim 122 wherein said at least one incoming data signal path is an address signal path.

133. The logic device of claim 122 wherein said at least one incoming data signal path is a command signal path.

134. The logic device of claim 122 wherein said at least one incoming data signal path is a data bus signal path.

135. The logic device of claim 122 wherein said at least one incoming data signal path is an input line signal path.

136. The logic device of claim 122 wherein said calibration bit pattern is received and calibration operations are performed at power-up and reset of said logic device.

137. The logic device of claim 122 wherein said clock signal clocks data on at least one of a rising or falling edge of said clock signal.

138. The logic device of claim 122 wherein said clock signal clocks data on both rising and falling edges of said clock signal.

139. A digital logic system, comprising:

a first logic device;

a second logic device connected to said first logic device; and

a calibration circuit on at least one of said first and second logic devices, said calibration circuit comprising:

an incoming pattern signal path;

a pattern storage device;

at least one incoming data signal path;

at least one variable delay circuit, respectively provided in said incoming data signal path or a clock signal path;

a control logic circuit connected to receive a calibration pattern signal including a calibration bit pattern on said incoming pattern signal path and store said calibration bit pattern in said pattern storage device, said control logic circuit subsequently using said stored calibration bit pattern and a clock signal during calibration operations to adjust said variable delay circuit to a delay value which produces a reliable detection of said stored calibration bit pattern within a calibration data signal received on said at least one incoming data signal path.

140. The logic system of claim 139 wherein said calibration circuit further comprises a repeater circuit that produces a repeating calibration signal using said stored calibration bit pattern.

141. The logic system of claim 139, further comprising a comparator circuit which compares bit patterns with said calibration data signal received on said at least one incoming data signal path with said stored calibration pattern during calibration operations, said control logic circuit using an output of said comparator circuit to determine said reliable detection of said stored calibration bit pattern.

142. The logic system of claim 139, further comprising a calibration circuit on at least said first logic device and said second logic device.

143. The logic system of claim 139 wherein said calibration pattern signal is received on said incoming pattern signal path at a first data rate slower than a normal operating data rate of said logic circuit.

144. The logic system of claim 143 wherein said calibration data signal is received on said at least one incoming data signal path at a second data rate approximately equal to said normal operating rate of said logic circuit.

145. The logic system of claim 143 wherein said calibration signal is received on said at least one incoming data signal path at a second data rate slower than or approximately equal to said normal operating rate of said logic circuit.

146. The logic system of claim 145 wherein said normal operating data rate of said logic circuit is about four times as fast as said first data rate.

147. The logic system of claim 145 wherein said normal operating data rate of said logic circuit is about eight times as fast as said first data rate.

148. The logic system of claim 139 wherein said calibration pattern is received from a data bus connected to said incoming pattern signal path.

149. The logic system of claim 139 wherein said calibration pattern is received from a command or address bus connected to said incoming pattern signal path.

150. The logic system of claim 139 wherein said at least one incoming data signal path is an address signal path.

151. The logic system of claim 139 wherein said at least one incoming data signal path is a command signal path.

152. The logic system of claim 139 wherein said at least one incoming data signal path is a data bus signal path.

153. The logic system of claim 139 wherein said at least one incoming data signal path is an input line signal path.

154. The logic system of claim 139 wherein said calibration bit pattern is received and calibration operations are performed at power-up and reset of said logic circuit.

155. The logic system of claim 139 wherein said clock signal clocks data on at least one of a rising or falling edge of said clock signal.

156. The logic system of claim 139 wherein said clock signal clocks data on both rising and falling edges of said clock signal.

157. The logic system of claim 139 wherein said pattern storage device stores only every Nth bit received on said incoming pattern signal path.

158. The logic system of claim 139 wherein said pattern storage device stores every bit received on said incoming pattern signal path, wherein only every Nth bit stored in said pattern storage device is used by said control logic circuit during calibration operations.

159. The logic system of claim 139 further comprising a prefetch demultiplexer that shifts only every Nth bit incoming to said pattern storage device.

160. The logic system of claim 139 wherein said calibration circuit further comprises a linear address counter that counts only every Nth address,

wherein said control logic circuit uses said linear address counter to retrieve only every Nth bit stored in said pattern storage device during calibration operations.

161. The logic system of claim 139 wherein said calibration circuit further comprises a test mode circuit that counts only every Nth address, wherein said control logic circuit uses said test mode circuit to retrieve only every Nth bit stored in said pattern storage device during calibration operations.

162. The logic system of claim 143 wherein said first data rate slower than said normal operating rate is achieved by lowering a frequency of a clock signal used to clock receipt of said calibration pattern.

163. The logic system of claim 139 further comprising a delay locked loop (DLL) circuit that is deactivated at least during receipt of said calibration bit pattern on said incoming pattern signal path.

164. The logic system of claim 139 further comprising a phase locked loop (PLL) circuit that is deactivated at least during receipt of said calibration bit pattern on said incoming pattern signal path.

165. The logic system of claim 139 further comprising a BIOS from which said calibration bit pattern is received on said incoming pattern signal path.

166. The logic system of claim 139 further comprising a ROM from which said calibration bit pattern is received on said incoming pattern signal path.

167. The logic system of claim 139 further comprising a network connection from which said calibration bit pattern is received on said incoming pattern signal path.

168. The logic system of claim 139 further comprising a command or address bus from which said calibration bit pattern is received on said incoming pattern signal path.

169. The logic system of claim 139 further comprising a data bus from which said calibration bit pattern is received on said incoming pattern signal path, wherein said calibration data signal is received on said incoming data signal path from said data bus.

170. A processor system, comprising:

a processor; and

an integrated memory circuit connected to said processor, at least one of said integrated memory circuit and processor including at least one calibration circuit comprising:

a incoming pattern signal path;

a pattern storage device;

at least one incoming data signal path;

at least one variable delay circuit, respectively provided in said incoming data signal path or a clock signal path;

a control logic circuit connected to receive a calibration pattern on said incoming pattern signal path and store said calibration pattern in said pattern storage device, said control logic circuit subsequently using said stored calibration pattern and a clock signal during calibration operations to adjust said variable delay circuit to a delay value which produces a reliable detection of said calibration pattern within a calibration signal received on said at least one incoming data signal path.

171. The processor system of claim 170 wherein at least said processor includes said calibration circuit.

172. The processor system of claim 170 wherein at least said integrated memory circuit includes said calibration circuit.

173. The processor system of claim 170 wherein said calibration circuit further comprises a repeater circuit that produces a repeating calibration signal that includes said calibration pattern.

174. The processor system of claim 173 wherein said calibration circuit is on each of a first and second logic devices and wherein a first calibration pattern signal including said calibration bit pattern is produced at said repeater circuit of said second logic device and applied to at least one data path of said first logic device, said control logic circuit of said first logic device using said stored calibration pattern, said applied first calibration signal and said clock signal to adjust a relative timing of clock and data signals on at least one data path of said

first logic device to produce a reliable detection of said calibration bit pattern on said at least one data path of said first logic device.

175. The processor system of claim 174 wherein a second calibration data signal including said calibration bit pattern is produced at said repeater circuit of said first logic device and applied to at least one data path of said second logic device, said control logic circuit of said second logic device using said stored calibration bit pattern, said applied second calibration signal and said clock signal at said second logic device to adjust a delay element in said at least one data path of said second logic device to a delay value which produces a reliable detection of said stored calibration pattern on said at least one data path of said second logic device.

176. The processor system of claim 170, further comprising a comparator circuit which compares bit patterns within said calibration data signal received on said at least one incoming data signal path with said stored calibration pattern during calibration operations, said control logic circuit using an output of said comparator circuit to determine said reliable detection of said stored calibration bit pattern.

177. The processor system of claim 170 wherein said calibration bit pattern is received on said incoming pattern signal path at a first data rate slower than a normal operating data rate of said logic circuit.

178. The processor system of claim 170 wherein said calibration data signal is received on said at least one incoming data path at a second data rate approximately equal to said normal operating rate of said logic circuit.

179. The processor system of claim 170 wherein said calibration data signal is received on said at least one incoming data path at a second data rate slower than or approximately equal to said normal operating rate of said logic circuit.

180. The processor system of claim 179 wherein said normal operating data rate of said logic circuit is about four times as fast as said first data rate.

181. The processor system of claim 179 wherein said normal operating data rate of said logic circuit is about eight times as fast as said first data rate.

182. The processor system of claim 170 wherein said pattern storage device stores only every Nth bit received on said incoming pattern signal path.

183. The processor system of claim 170 wherein said pattern storage device stores every bit received on said incoming pattern signal path, wherein only every Nth bit stored in said pattern storage device is used by said control logic circuit during calibration operations.

184. The processor system of claim 170 wherein said calibration circuit further comprises a linear address counter that counts only every Nth address,

wherein said control logic circuit uses said linear address counter to retrieve only every Nth bit stored in said pattern storage device during calibration operations.

185. The processor system of claim 170 wherein said calibration circuit further comprises a test mode circuit that counts only every Nth address, wherein said control logic circuit uses said test mode circuit to retrieve only every Nth bit stored in said pattern storage device during calibration operations.

186. The processor system of claim 177 wherein said first data rate slower than said normal operating rate is achieved by lowering a frequency of a clock signal used to clock receipt of said calibration pattern.